# به نام خدا

تمرین دوم

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استاد : دکتر صاحب الزمانی

سوال 8 :

کد این سوال به صورت زیر است :

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

entity GrayCode is Port (

clk : in std\_logic ;

reset : in std\_logic ;

counter : out std\_logic\_vector(3 downto 0)

);

end GrayCode;

architecture RTL of GrayCode is

signal temp : std\_logic\_vector(3 downto 0);

begin

process(clk)

begin

if( clk'event and clk = '1') then

if( reset = '1' )then

temp <= "0000";

else

case temp is

when "0000" => temp <= "0001";

when "0001" => temp <= "0011";

when "0011" => temp <= "0010";

when "0010" => temp <= "0110";

when "0110" => temp <= "0111";

when "0111" => temp <= "0101";

when "0101" => temp <= "0100";

when "0100" => temp <= "1100";

when "1100" => temp <= "1101";

when "1101" => temp <= "1111";

when "1111" => temp <= "1110";

when "1110" => temp <= "1010";

when "1010" => temp <= "1011";

when "1011" => temp <= "1001";

when "1001" => temp <= "1000";

when "1000" => temp <= "0000";

when others => temp <= "0000";

end case;

end if;

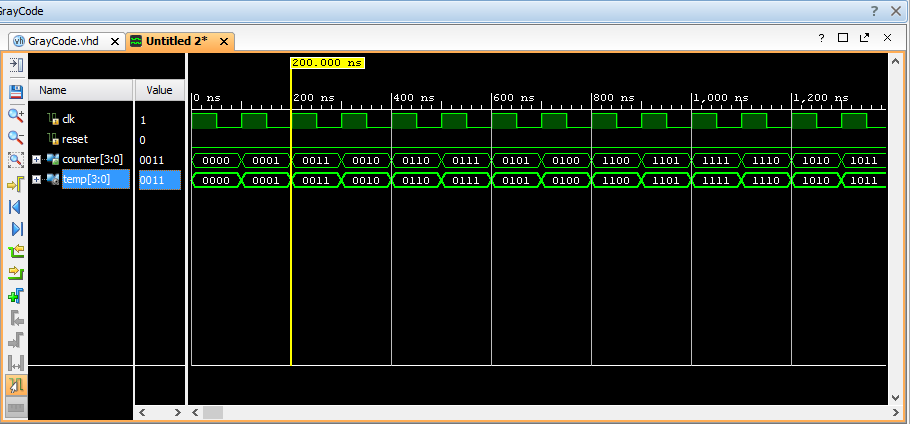
end if;

end process;

counter <= temp;

end RTL;

شکل موج آن به صورت زیر میباشد :



سوال 9 :

کد آن به صورت زیر است :

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.std\_logic\_unsigned.ALL;

entity RippleCounter is

generic (

n : natural := 4

);

port (

clk : in std\_logic;

reset : in std\_logic;

counter : out std\_logic\_vector(n-1 downto 0)

);

end RippleCounter;

architecture RTL of RippleCounter is

signal clk\_arr, counter\_arr : std\_logic\_vector(n-1 downto 0);

begin

clk\_arr(0) <= clk;

clk\_arr(n-1 downto 1) <= counter\_arr(n-2 downto 0);

gen\_cnt: for i in 0 to n-1 generate

dff: process(reset , clk\_arr(i))

begin

if (reset = '1') then

counter\_arr(i) <= '1';

elsif (clk\_arr(i)'event and clk\_arr(i) = '1') then

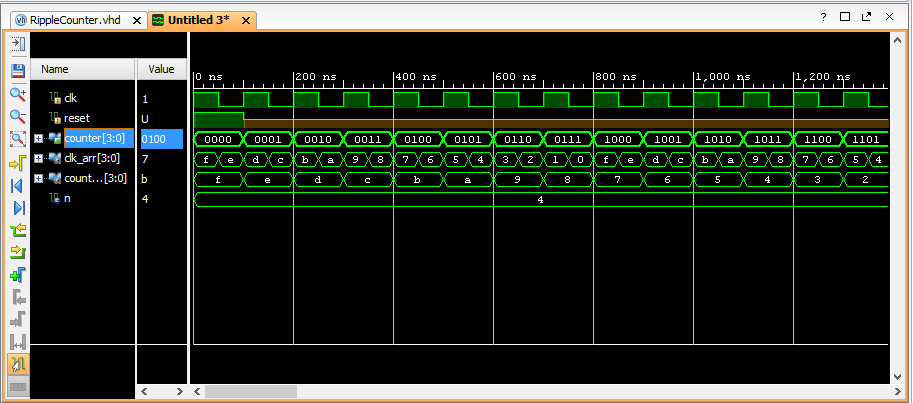
counter\_arr(i) <= not counter\_arr(i);

end if;

end process dff;

end generate;

شکل موج آن به صورت زیر می باشد :



سوال 10 :

با توجه به اینکه در process آخرین ASSIGNMENT در PROCESS اجرا میشود مقدار X برابر 1 و مقدار Y برابر 0 خواهد ماند . همچنین W چون هیچ گاه تغییر نمیکند برابر همان مقدار اولیه یعنی u میماند.Z هم با توجه به تنها انتسابش برابر 1 خواهد بود.

سوال 11 :

Configuration conf\_name of my\_module is

for arch\_name

For MODULE1:M1

Use entity work.multiplier(sequential);

End for;

For others:M1

Use entity work.multiplier(array)

End for;

End for;

End conf\_name;

سوال 12 :

کد این سوال برای هر سه قسمت برابر زیر است :

library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

use IEEE.std\_logic\_unsigned.ALL;

use ieee.numeric\_std.all;

entity temprature is Port (

temp1 : in std\_logic\_vector( 7 downto 0 ) ;

temp2 : in std\_logic\_vector( 7 downto 0 ) ;

temp3 : in std\_logic\_vector( 7 downto 0 ) ;

temp4 : in std\_logic\_vector( 7 downto 0 ) ;

temp5 : in std\_logic\_vector( 7 downto 0 ) ;

cooler : out bit ;

heater : out bit );

end temprature;

architecture concurrent of temprature is

signal avg : std\_logic\_vector( 7 downto 0 ) ;

begin

avg <= std\_logic\_vector(shift\_right(unsigned(temp1 + temp2 + temp3 + temp4) , natural(2)));

cooler <= '0' when avg < temp5 + 4 else

'0' when avg > temp5 - 4 and avg < temp5 + 4 else

'1';

heater <= '1' when avg < temp5 - 4 else

'0' when avg > temp5 - 4 and avg < temp5 + 4 else

'0';

end concurrent;

architecture sequential of temprature is

signal avg\_sig : std\_logic\_vector( 7 downto 0 ) ;

begin

process(temp1 , temp2 , temp3 , temp4 , temp5)

variable avg : std\_logic\_vector( 7 downto 0 ) ;

begin

avg := std\_logic\_vector(shift\_right(unsigned(temp1 + temp2 + temp3 + temp4) , natural(2)));

if( avg < temp5 - 4 ) then

heater <= '1' ;

cooler <= '0';

elsif( avg > temp5 - 4 and avg < temp5 + 4 ) then

heater <= '0';

cooler <= '0';

else

heater <= '0';

cooler <= '1';

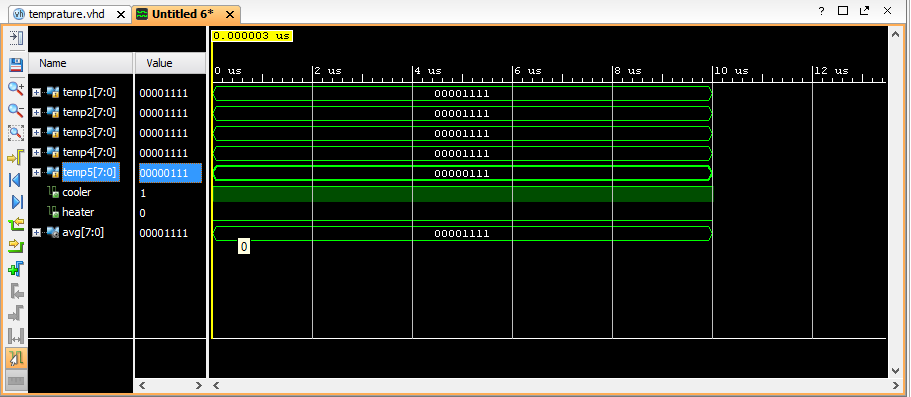
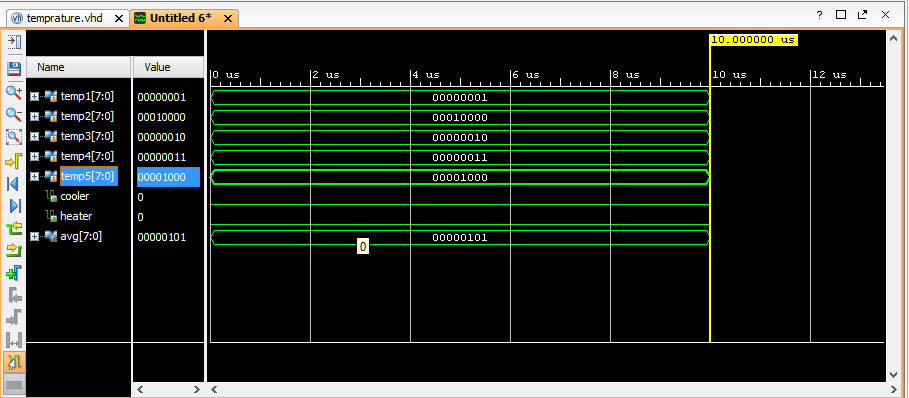
end if;

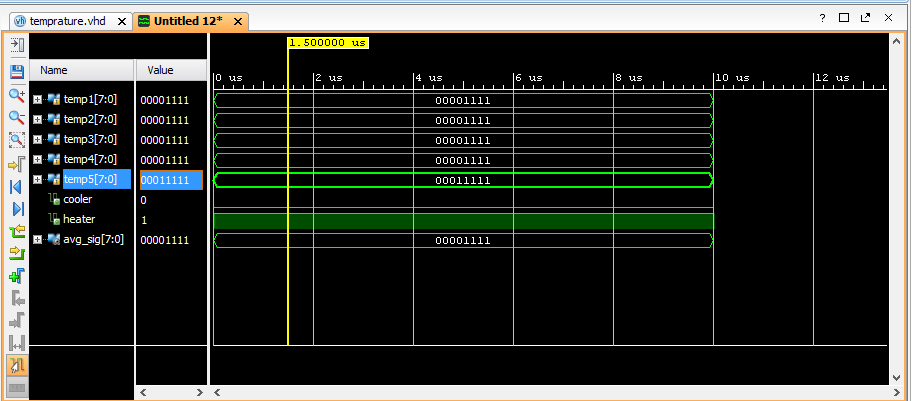
avg\_sig <= avg;

end process;

end sequential;

برای کد بالا شکل موج های زیر تولید شده است :





سوال 13 :

کد این مدار به صورت زیر است :

entity makaroni is Port (

pressure : in integer ;

output : out std\_logic\_vector( 1 downto 0)

);

end makaroni;

architecture Behavioral of makaroni is

begin

output <= "00" when pressure >= 5 and pressure <= 10 else

"01" when pressure > 10 and pressure <= 15 else

"10" when pressure > 15 and pressure <= 20 else

"11" when pressure > 20 and pressure <= 25 else

"00";

with pressure select

output <= "00" when 5 to 10,

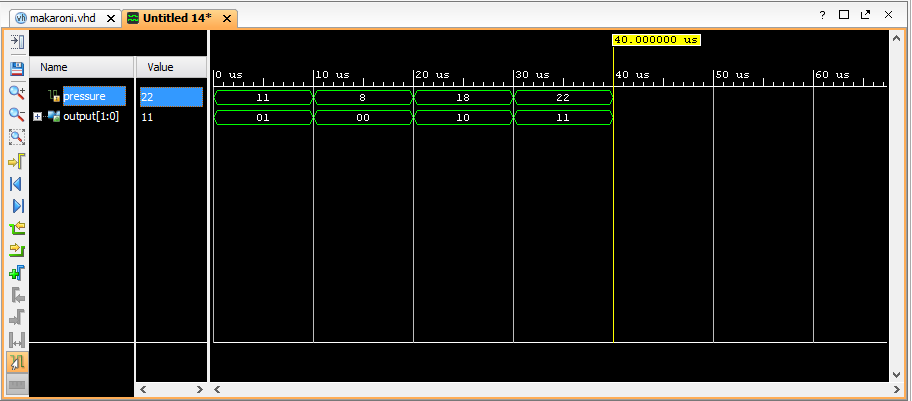
"01" when 11 to 15,

"10" when 16 to 20,

"11" when 21 to 25,

"00" when others;

end Behavioral;

شکل موج آن به صورت زیر است :

سوال 14 :

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-- Company:

-- Engineer:

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-- Create Date: 03/02/2017 02:14:36 PM

-- Design Name:

-- Module Name: frequency\_divider - Behavioral

-- Project Name:

-- Target Devices:

-- Tool Versions:

-- Description:

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-- Dependencies:

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-- Revision:

-- Revision 0.01 - File Created

-- Additional Comments:

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library IEEE;

use IEEE.STD\_LOGIC\_1164.ALL;

-- Uncomment the following library declaration if using

-- arithmetic functions with Signed or Unsigned values

--use IEEE.NUMERIC\_STD.ALL;

-- Uncomment the following library declaration if instantiating

-- any Xilinx leaf cells in this code.

--library UNISIM;

--use UNISIM.VComponents.all;

use IEEE.numeric\_std.ALL;

entity frequency\_divider is

generic (N : integer := 10 );

port (

clk,reset : in std\_logic;

clk\_out : out std\_logic);

end frequency\_divider;

architecture Behavioral of frequency\_divider is

signal count: integer:=0;

signal tmp : std\_logic := '1';

begin

process(clk,reset)

begin

if(reset='0') then

count<=0;

tmp<='1';

elsif(clk'event and clk='1') then

count <=count+1;

if (count = N) then

tmp <= NOT tmp;

count <= 0;

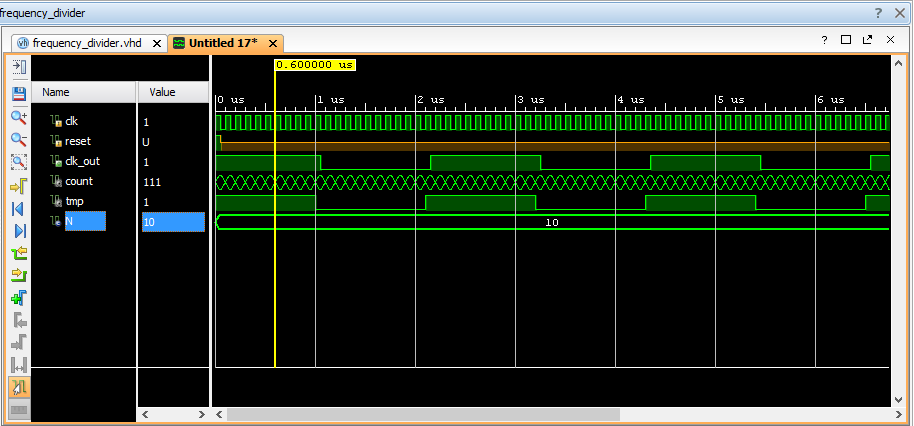
end if;

end if;

clk\_out <= tmp;

end process;

end Behavioral;

شکل موج آن به صورت زیر است :